CH7211A DisplayPort to HDMI 2.0 Converter on USB Type C

FEATURES

- Compliant with DisplayPort Alternate Mode on USB Type C standard
- Compliant with DisplayPort Specification version 1.3 and Embedded DisplayPort (eDP) Specification version 1.4
- Support up to 4 Main Link Lanes at 1.62Gbps,2.7Gbps (HBR) or 5.4Gbps (HBR2) link rate
- Automotive DP input signal detection and Lane swap supported for compliance with the USB type C cable plug orientation switch
- DP_BR signaling modes supported
- Programmable DisplayPort receiver equalization supported for the compensation of input signal attenuation
- Support Spread Spectrum Clocking (de-spreading) for EMI reduction
- Support Fast and full Link Training
- Support eDP Authentication: Alternative Scramble Seed Reset and Alternative Framing
- HDMI transmitter compliant with HDMI specification version 2.0 and DVI specification version 1.0
- HDMI transmitter supports up to 6.0Gbps data rate for video timing of 4Kx2K@60Hz
- HDMI 3D dual view and 3D audio are supported
- High-Dynamic-Range (HDR) display are supported
- YCC 4:4:4/4:2:2 to YCC 4:2:2/4:2:0,Y-only(Gray display) conversion are supported
- HDCP engine compliant with HDCP 2.2 specification with internal HDCP Keys
- HDCP 2.2 repeater supported
- Active DDC buffer and related control register integrated
- SCDC supported on HDMI DDC
- IIC-over-AUX transaction supported
- CEC tunneling over AUX is supported
- AUX CH polarity inversion supported for USB type C cable plug orientation switch
- Programmable Pre-Emphasis on output driver supported
- Support 2 USB Type-C ports that are compliant with USB Type-C Cable and Connector Specification revision 1.3.
- Compliant with USB Power Delivery Specification Revision 3.0, Version 1.1, with USB Power Delivery BMC transceiver integrated on each USB Type-C port
- Integrated Ra, Rd and Rp for USB Type-C
- On-chip Audio Decoder which support 8 channel Audio input from DP Rx and output from HDMI Tx with sample rate up to 192KHz
- SPDIF/IIS input supported with audio sampling rate up to 192KHz
- Embedded MCU to handle the control logic
- Full speed USB billboard module integrated
- USB 2.0 PHY supported with internal switch for

GENERAL DESCRIPTION

Chrontel's CH7211A is a low-cost, low-power semiconductor device that translates the DisplayPort signal to HDMI/DVI through the USB Type-C connector. This innovative USB Type-C based DisplayPort receiver with an integrated HDMI Transmitter is specially designed to target the USB Type-C to HDMI converter, adopter and docking device. Through the CH7211A's advanced decoding / encoding algorithm, the input DisplayPort high-speed serialized multimedia data can be seamlessly converted to HDMI/DVI output.

The CH7211A's DP/eDP receiver is compliant with the DisplayPort Specification 1.3 and Embedded DisplayPort (eDP) Specification version 1.4. With sophisticated DisplayPort signal detection and the Lane Swap/AUX polarity inversion logic, the CH7211A supports USB Type-C cable plug orientation switch. With internal HDCP key Integrated, the device support HDCP 2.2 specifications. In the device's receiver block, which supports four DisplayPort Main Link Lanes input with data rate running at 1.62Gbps, 2.7Gbps or 5.4Gbps, and converted the input signal to HDMI output up to 4Kx2k@60Hz. Leveraging the USB Power Delivery control logic, the USB billboard module for USB device indentify and DisplayPort's unique source/sink "Link Training" routine, the CH7211A is capable of instantly bring up the video display to the HDMI/DVI TV/Monitor when the initialization process is completed.

The CH7211A also supports up to 8-channel audio input from either DP Rx or SPDIF port and output from HDMI Tx with sample rate up to 192 KHz. Available audio bandwidth depends on the pixel clock frequency, the video format timing, and whether or not content protection re-synchronization is needed.

With sophisticated MCU and the embedded EEPROM, CH7211A support auto-boot and EDID buffer. Leveraging the firmware auto-loaded from the embedded EEPROM, CH7211A can support DP input detection, HDMI connection detection, and determine to enter into Power saving mode automatically.

data/file transport in USB full speed mode
- Embedded EEPROM, integrated EDID Buffer
- IIC Slave, USB 2.0 are available for firmware update
- IIC slave interface are available for debug
- Support Auto Power Saving mode and low stand-by current
- Anti-back drive support
- Low power architecture
- RoHS compliant and Halogen free package
- HBM 2KV ESD performance
- Offered in 64 pin QFN package

APPLICATION

- USB Type C to HDMI 2.0 cable/Adapter/Docking Station
- On-board DP to HDMI 2.0 application
- USB Type-C Monitor/Projector/Display

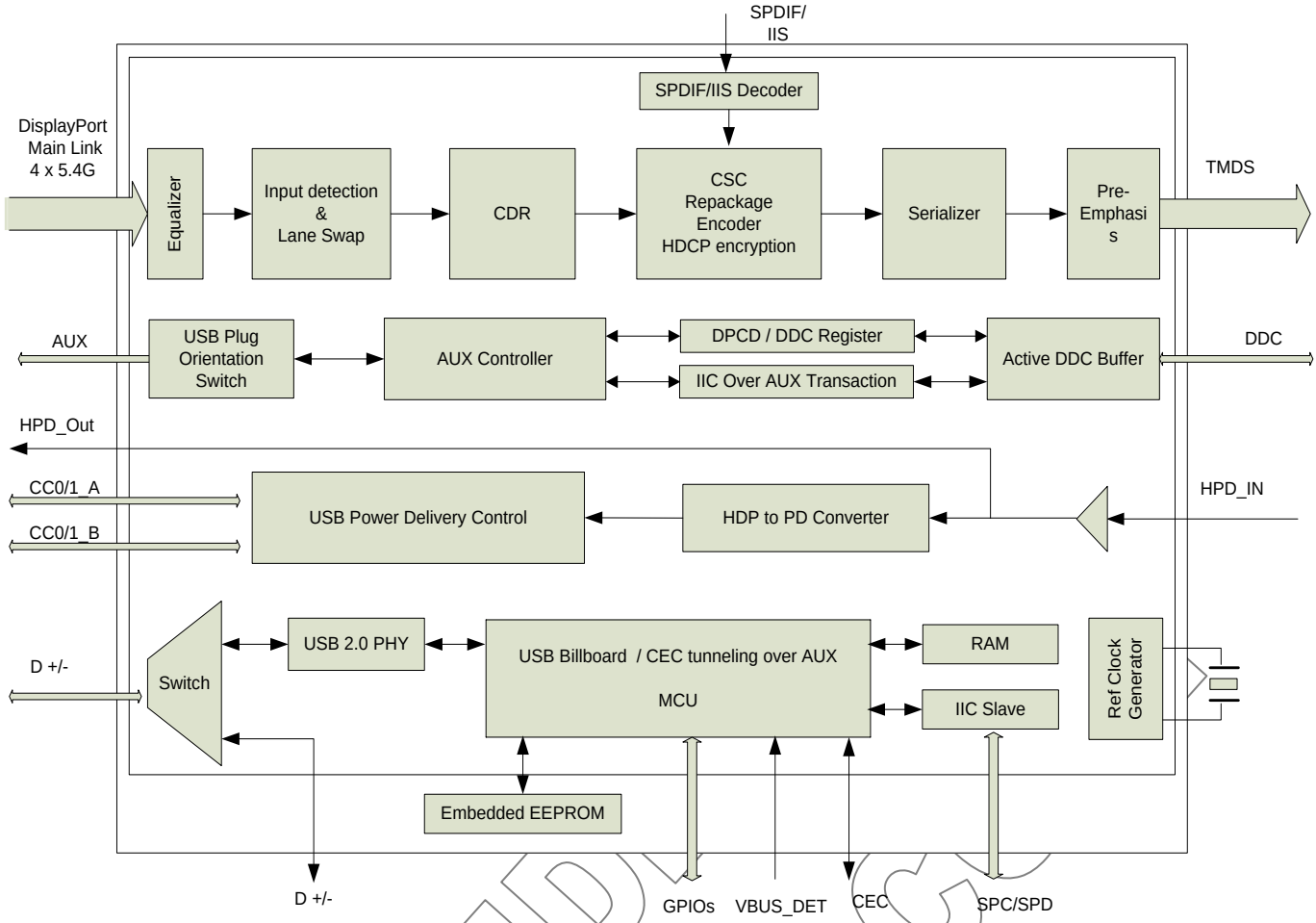

Figure 1: CH7211A Functional Block Diagram

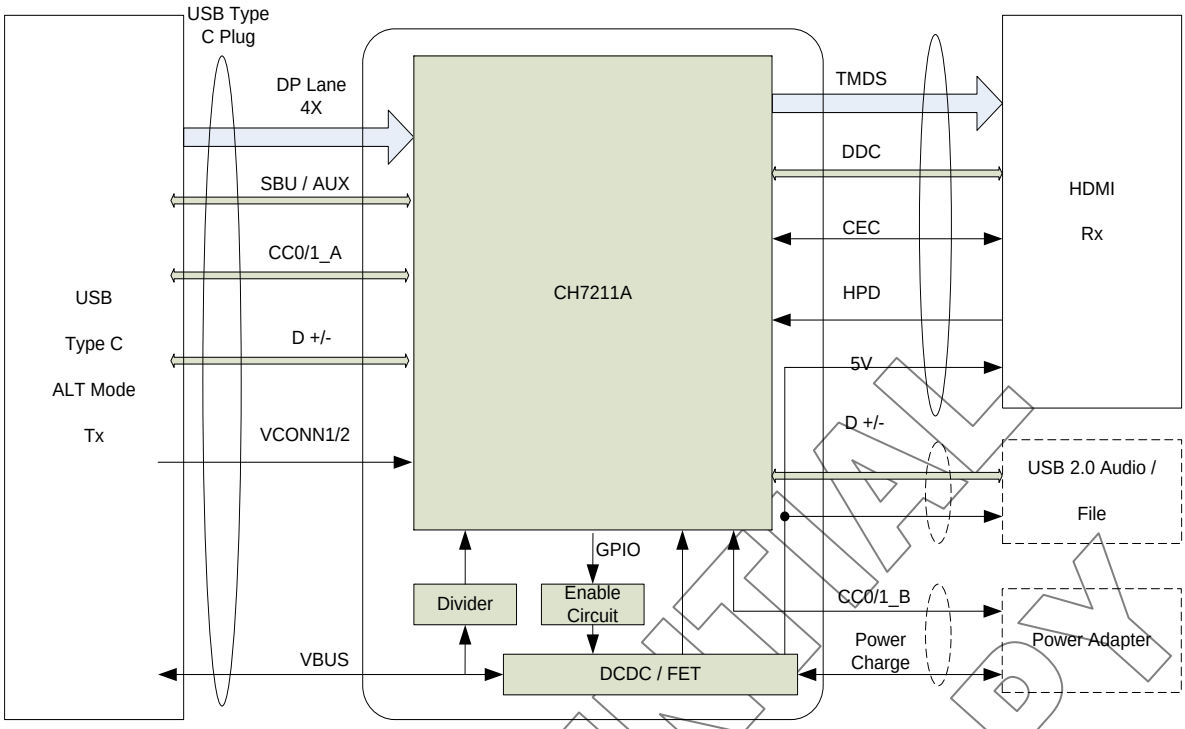

Figure 2: CH7211A USB Type-C to HDMI / USB 2.0 / Power Charge Docking Application Block Diagram

1.0 PIN-OUT

1.1 Package Diagram

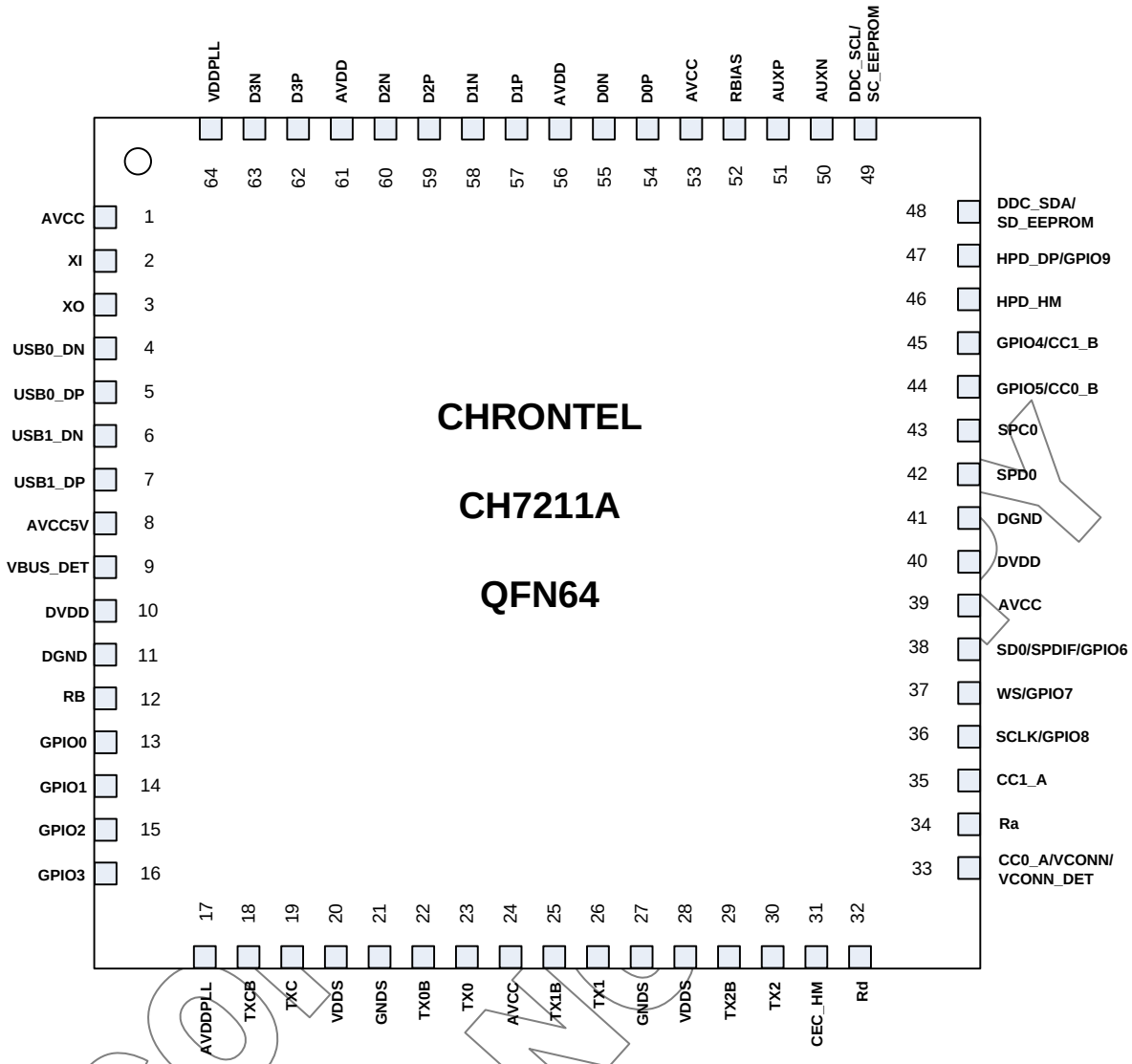

Figure 3: CH7211A 64-Pin QFN Pin Out

1.2 Pin Description

Table 1: 64 BGA Pin Name Descriptions

Pin #	Type	Symbol	Description
2	In	XI	**Crystal Input / External Reference Input** A parallel resonance crystal should be attached between this pin and XO. An external 3.3V CMOS compatible clock also can drive the XI Input
3	Out	XO	**Crystal Output** A parallel resonance crystal should be attached between this pin and XI / FIN. However, if an external CMOS clock is attached to XI/FIN, XO should be left open
4,5	In/Out	USB0_DN/ USB0_DP	**D+/- Input of USB Type C Interface**
6,7	In/Out	USB1_DN/ USB1_DP	**USB 2.0 Output Pins**
9	In	VBUS_DET	**USB VBUS Voltage Detection** Voltage input 0 ~ 5V
12	In	RB	**Reset* Input (Internal pull-up)** When this pin is low, the device is held in the power-on reset condition. When this pin is high, reset is controlled through the serial port register.
13~16	In/Out	GPIO[3:0]	**General Purpose Input/Output Interface**
18,19	Out	TXCB/ TXC	**HDMI Clock Outputs** These pins provide the differential clock output for the HDMI
22,23	Out	TX0B/ TX0	**HDMI Data Channel 0 Outputs** These pins provide the TMDS differential outputs for data channel 0
25,26	Out	TX1B/ TX1	**HDMI Data Channel 1 Outputs** These pins provide the TMDS differential outputs for data channel 1
29/30	Out	TX2B/ TX2	**HDMI Data Channel 2 Outputs** These pins provide the TMDS differential outputs for data channel 2
31	In/Out	CEC_HM	**HDMI CEC Channel**
32	In	Rd	**USB Type-C Dead Battery Rd Resistor** Connect CC0_A to this pin to enable dead battery Rd on CC0_A pin
33	In/Out	CC0_A	**Port A USB Type-C Configure Channel 0**
	In	VCONN	**VCONN Input** Connect this pin to VCONN pin of USB Type-C Plug Connector if CH7211A is used in VCONN Power Accessory mode.
	In	VCONN_DET	**USB VCONN Voltage Detection** Voltage input 2.7 ~ 5.5v
34	In	Ra	**Ra Resistor** When used in typeC accessory mode, this pin needs connect to CC0.
35	In/Out	CC1_A	**Port A USB Type-C Configure Channel 1**
36	In	SCLK	**IIS Audio Input's Bit clock**
	In/Out	GPIO8	**General Purpose Input/Output Interface**
37	In	WS	**IIS Audio Input's WS**
	In/Out	GPIO7	**General Purpose Input/Output Interface**
38	In	SD0/SPDIF	**IIS Audio Input's Data or SPDIF Input.**
	In/Out	GPIO6	**General Purpose Input/Output Interface**
42	In/Out	SPD0	**Serial Port Data Input / Output** This pin functions as the bi-directional data pin of the serial port. External pull-up 6.8 KΩ resister is required

43	In	SPC0	**Serial Port Clock Input** This pin functions as the clock pin of the serial port. External pull-up 6.8 KΩ resister is required
44	In/Out	CC0_B	**Port B USB Type-C Configure Channel 0**
	In/Out	GPIO5	**General Purpose Input/Output**
45	In/Out	CC1_B	**Port B USB Type-C Configure Channel 1**
	In/Out	GPIO4	**General Purpose Input/Output**
46	In	HPD_HM	**HDMI Tx HPD Input**
47	Out	HPD_DP	**DP Rx HPD Output**
	In/Out	GPIO9	**General Purpose Input/Output**
48	In	DDC_SDA	**Serial Port Data to HDMI Receiver** The pin should be connected to data signal of HDMI DDC. This pin requires a pull-up 1.8 kΩ resistor to the desired voltage level
	In/Out	SD_EEPROM	**Connect to External EEPROM I2C Port Data** The EEPROM is optional depending on FW size
49	Out	DDC_SCL	**Serial Port Clock Output to HDMI Receiver** The pin should be connected to clock signal of HDMI DDC. This pin requires a pull-up 1.8kΩ resistor to the desired voltage level
	Out	SC_EEPROM	**Connect to External EEPROM I2C Port Clock**
50,51	In/Out	AUXN/AUXP	**AUX Channel Differential Input/Output** These two pins are DisplayPort AUX Channel control, which supports a half-duplex, bi-directional AC-coupled differential signal.
52	In	RBIAS	**HDMI Swing Control** This pin sets the swing level of the HDMI outputs. A 1K-ohm with 1% tolerance resistor should be connected between this pin and ground using short and wide traces.
54,55	In	D0P/ D0N	**DP Main Link Differential Lane 0 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
57/58	In	D1P/ D1N	**DP Main Link Differential Lane 1 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
59,60	In	D2P/ D2N	**DP Main Link Differential Lane 2 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
62,63	In	D3P/ D3N	**DP Main Link Differential Lane 3 Input** These pins accept four AC-coupled differential pair signals from the DisplayPort transmitter.
1,24,39,53	Power	AVCC	**Analog Power Supply(3.3V)**
8	Power	AVCC5V	**Analog Power Supply (5V)**
10,40	Power	DVDD	**Digital Core/IO Power Supply (1.2V)**
11,41	Power	DGND	**Digital Ground**
17	Power	AVDDPLL	**PLL Power Supply (1.2V)**
20,28	Power	VDDS	**Serializer Power Supply (1.2V)**
21,27	Power	GNDS	**Ground**
56,61	Power	AVDD	**Analog Power Supply (1.2V)**
64	Power	VDDPLL	**PLL Power Supply (1.2V)**

2.0 PACKAGE DIMENSION

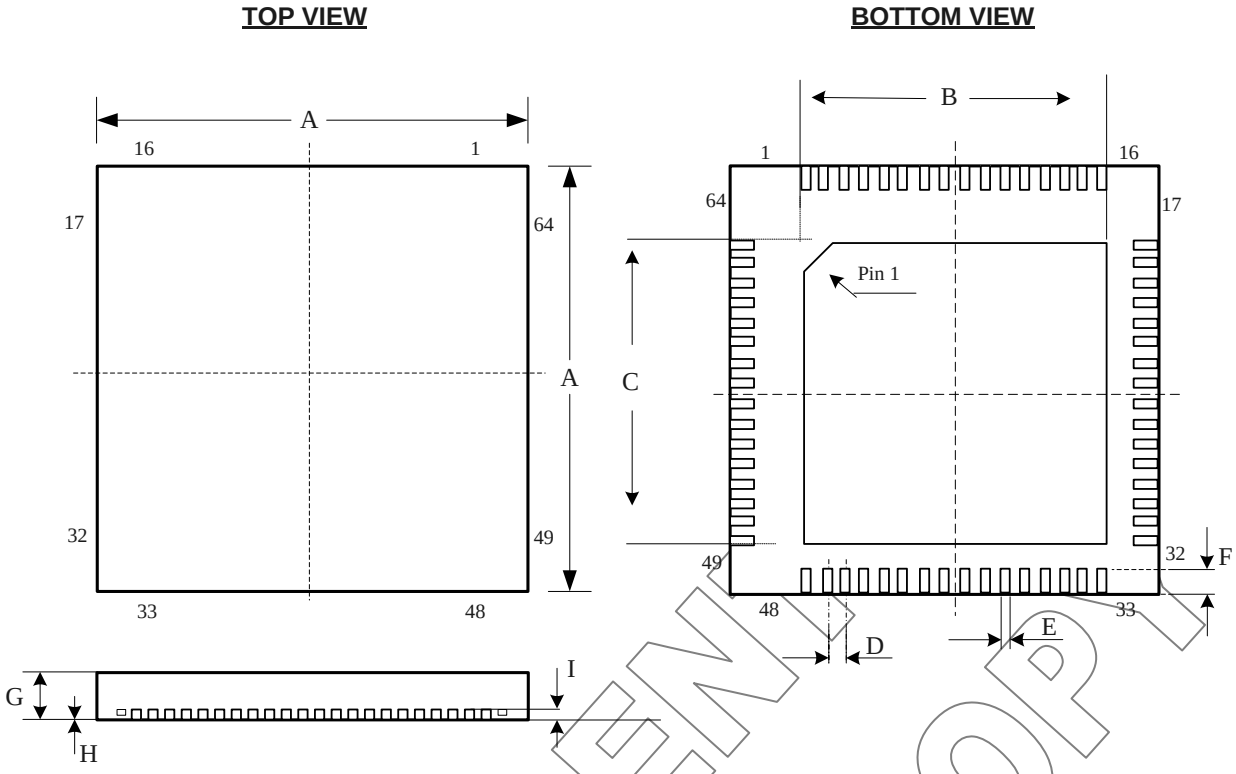

Figure 4: 64 Pin QFN Package (8x8 mm)

Table of Dimensions

No. of Leads		SYMBOL								
64 (8x8 mm)		A	B	C	D	E	F	G	H	I
Milli-meters	MIN	7.90	6.10	6.10	0.40 BSC	0.15	0.35	0.70	0.00	0.203 REF
	MAX	8.10	6.30	6.30		0.25	0.45	0.80	0.05	

Notes:

1. All dimensions conform to JEDEC standard MO-207.

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ORDERING INFORMATION				
Part Number	**Package Type**	**Content Protection**	**Operating Temperature Range**	**Minimum Order Quantity**
CH7211A-BF	64 QFN, Lead-free	None	Commercial : 0 to 70°C	**260/Tray**
CH7211A-BFK	64 QFN, Lead-free	HDCP 2.2	Commercial : 0 to 70°C	**260/Tray**

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